Voltage Comparator

FEATURES

- Pin-Compatible with LM111 Series Devices
- *Guaranteed* Max. 0.5mV Input Offset Voltage
- *Guaranteed* Max. 25nA Input Bias Current
- *Guaranteed* Max. 3nA Input Offset Current
- *Guaranteed* Max. 250ns Response Time
- *Guaranteed* Min. 200,000 Voltage Gain
- 50mA Output Current Source or Sink
- ±30V Differential Input Voltage
- Fully Specified for Single +5V Operation

APPLICATIONS

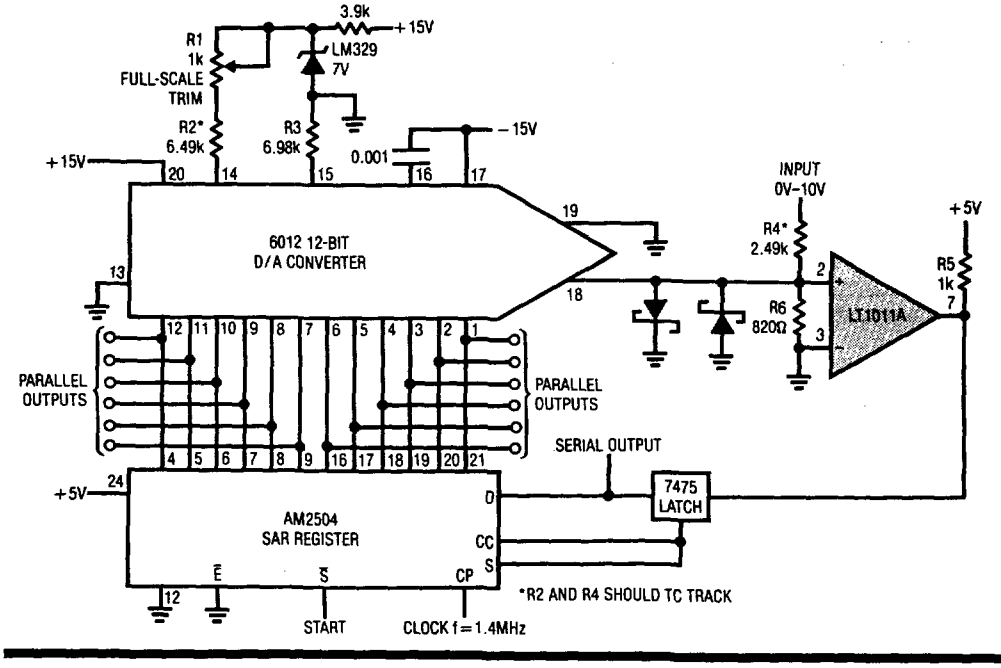
- SAR A to D Converters
- Voltage to Frequency Converters
- Precision R/C Oscillator
- Peak Detector
- Motor Speed Control
- Pulse Generator
- Relay/Lamp Driver

DESCRIPTION

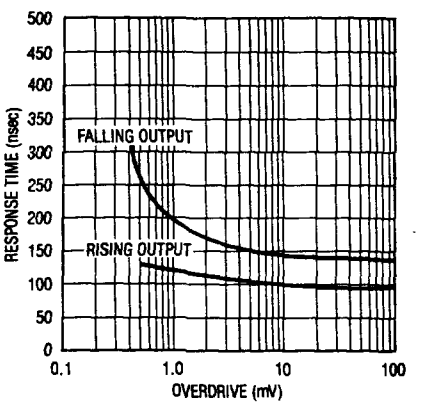
The LT1011 is a general purpose comparator with significantly better input characteristics than the LM111. Although pin-compatible with the LM111, it offers four times lower bias current, six times lower offset voltage, and five times higher voltage gain. Offset voltage drift—a previously unspecified parameter—is guaranteed at 15μV/°C. Additionally, the supply current is lower by a factor of two with no loss in speed. The LT1011 is several times faster than the LM111 when subjected to large overdrive conditions. It is also fully specified for DC parameters and response time when operating on a single +5V supply. These parametric improvements allow the LT1011 to be used in high accuracy (≥12-bit) systems without trimming. In a 12-bit A to D application, for instance, using a 2mA DAC, the offset error introduced by the LT1011 is less than 1/2 LSB. The LT1011 retains all the versatile features of the LM111, including single 3V to ±18V supply operation, and a floating transistor output with 50mA source/sink capability. It can drive loads referenced to ground, negative supply or positive supply, and is specified up to 50V between V⁻ and the collector output. A differential input voltage up to the full supply voltage is allowed, even with ±18V supplies, enabling the inputs to be clamped to the supplies with simple diode clamps.

6

10μs 12-Bit A-D Converter



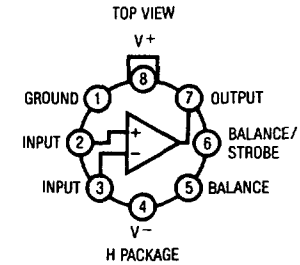
Response Time vs Overdrive



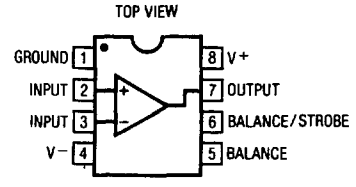
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (pin 8 to pin 4) 36V
Output to Negative Supply (pin 7 to pin 4)
LT1011AM, LT1011M 50V
LT1011AC, LT1011C 40V
Ground to Negative Supply
(pin 1 to pin 4) 30V
Differential Input Voltage ..... ±36V
Voltage at Strobe Pin (pin 6 to pin 8) 5V
Input Voltage (Note 1) ..... Equal to Supplies
Output Short Circuit Duration ..... 10 sec.
Operating Temperature Range (Note 2)
LT1011AM/LT1011M ..... −55°C to 125°C
LT1011AC/LT1011C ..... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION



H PACKAGE
TO-5 METAL CAN



NOTE: PIN 4 CONNECTED TO CASE.

J8 PACKAGE 8 PIN CERDIP
N8 PACKAGE 8 PIN PLASTIC

ORDER PART NUMBER
LT1011AMH LT1011MH LT1011ACH LT1011CH
LT1011AMJ8 LT1011MJ8 LT1011ACJ8 LT1011CJ8 LT1011ACN8 LT1011CN8

ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, $V_{CM} = 0V$, $R_S = 0$, $T_J = 25°C$, $V_I = -15V$, output at pin 7 unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1011AM/LT1011AC MIN	LT1011AM/LT1011AC TYP	LT1011AM/LT1011AC MAX	LT1011M/LT1011C MIN	LT1011M/LT1011C TYP	LT1011M/LT1011C MAX	UNITS
V_{OS}	Input Offset Voltage	Note 3			0.3	0.5		0.6	1.5	mV
			●			1.0			3.0	mV
V_{OS}	*Input Offset Voltage	$R_S \leq 50k\Omega$ (Note 4)				0.75			2.0	mV
			●			1.5			3.0	mV
I_{OS}	*Input Offset Current	Note 4			0.2	3		0.2	4	nA
			●			5			6	nA
I_b	Input Bias Current	Note 3			15	25		20	50	nA
I_b	*Input Bias Current	Note 4			20	35		25	65	nA
			●			50			80	nA
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage Drift (Note 5)	$T_{MIN} \leq T \leq T_{MAX}$	●		4	15		4	25	µV/°C
A_{VOL}	*Large Signal Voltage Gain	$R_L = 1k\Omega$ to $+15V$, $-10V \leq V_{OUT} \leq 14.5V$		200	500		200	500		V/mV
		$R_L = 500\Omega$ to $+5V$, $0.5V \leq V_{OUT} \leq 4.5V$		50	300		50	300		V/mV
CMRR	Common-Mode Rejection Ratio			94	115		90	115		dB
	*Input Voltage Range (Note 8)	$V_S = \pm 15V$	●	−14.5		13	−14.5		13	V
		V_S = Single +5V	●	0.5		3.0	0.5		3.0	V
T_d	*Response Time	Note 6			150	250		150	250	ns
V_{OL}	*Output Saturation Voltage	$V_{IN} = 5$ mV, $I_{SINK} = 8$mA	●		0.25	0.4		0.25	0.4	V
		$V_I = 0$, $I_{SINK} = 50$ mA	●		0.7	1.5		0.7	1.5	V
	*Output Leakage Current	$V_{IN} = 5$mV, $V1 = -15V$			0.2	10		0.2	10	nA
		$V_{OUT} = 35V$ (25V for LT1011C)	●			500			500	nA
	*Positive Supply Current				3.2	4.0		3.2	4.0	mA
	*Negative Supply Current				1.7	2.5		1.7	2.5	mA
	*Strobe Current	Minimum to Ensure Output Transistor is Off		500			500			µA
	Input Capacitance				6			6		pF

*indicates parameters which are guaranteed for all supply voltages, including a single 5V supply. See Note 4.

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Inputs may be clamped to supplies with diodes so that maximum input voltage actually exceeds supply voltage by one diode drop. See Input Protection in applications section.

Note 2: T_J max = 150°C for the LT1011AM/LT1011M and 95°C for the LT1011AC/LT1011C.

Note 3: Output is sinking 1.5mA with $V_{OUT} = 0V$.

Note 4: These specifications apply for all supply voltages from a single +5V to ±15V, the entire input voltage range, and for both high and low output states. The high state is $I_{SINK} \geq 100\mu A$, $V_{OUT} \geq (V^+ - 1V)$ and the low state is $I_{SINK} \leq 8mA$, $V_{OUT} \leq 0.8V$. Therefore, this specification defines a worst-case error band that includes effects due to common-mode signals, voltage gain, and output load.

Note 5: Drift is calculated by dividing the offset voltage difference measured at min and max temperatures by the temperature difference.

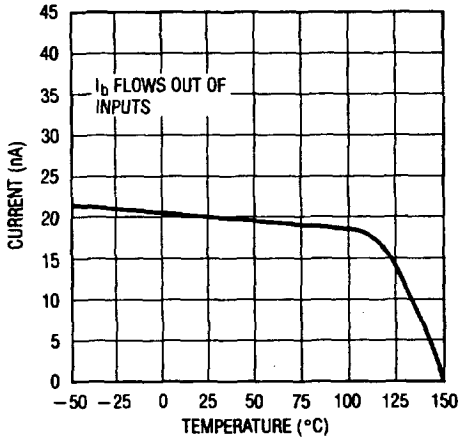
Note 6: Response time is measured with a 100mV step and 5mV overdrive. The output load is a 500Ω resistor tied to +5V. Time measurement is taken when the output crosses 1.4V.

Note 7: Do not short the strobe pin to ground. It should be current driven at 3mA to 5mA for the shortest strobe time. Currents as low as 500μA will strobe the LT111A if speed is not important. External leakage on the strobe pin in excess of 0.2μA when the strobe is "off" can cause offset voltage shifts.

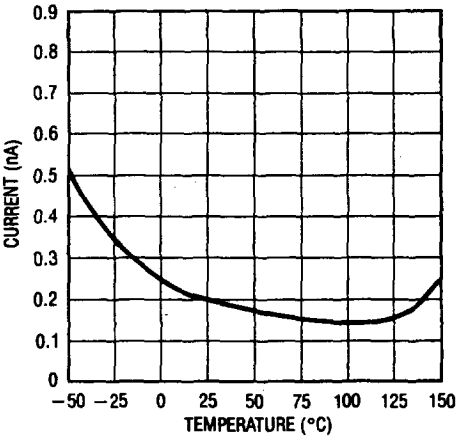
Note 8: See graph, Input Offset Voltage vs Common-Mode Voltage.

TYPICAL PERFORMANCE CHARACTERISTICS

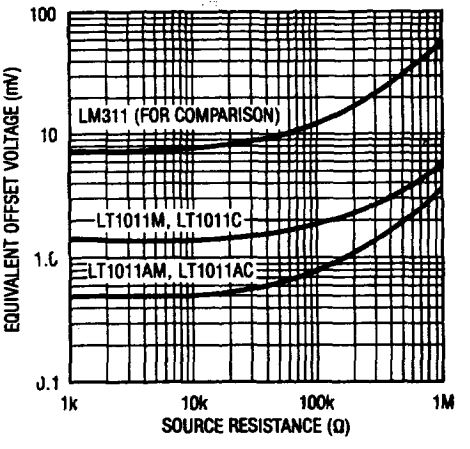
Input Bias Current



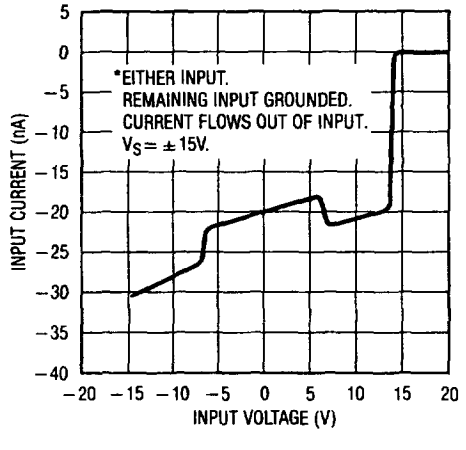
Input Offset Current



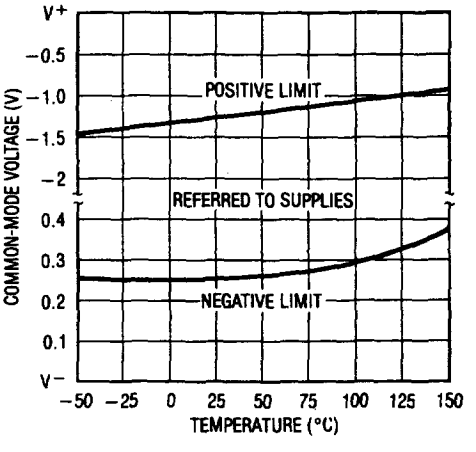
Worst-Case Offset Error



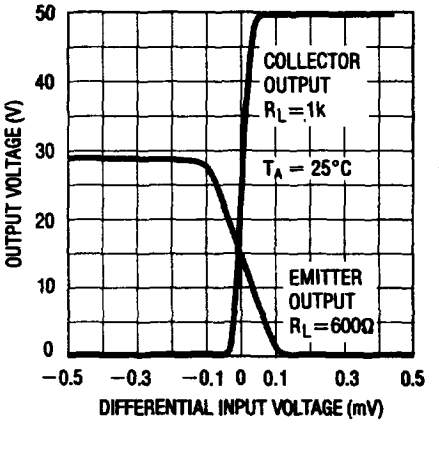
Input Characteristics*



Common-Mode Limits



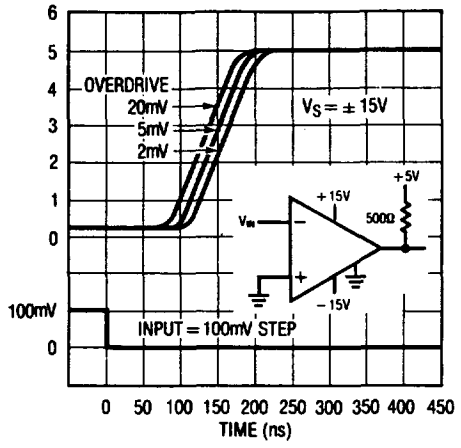
Transfer Function (Gain)



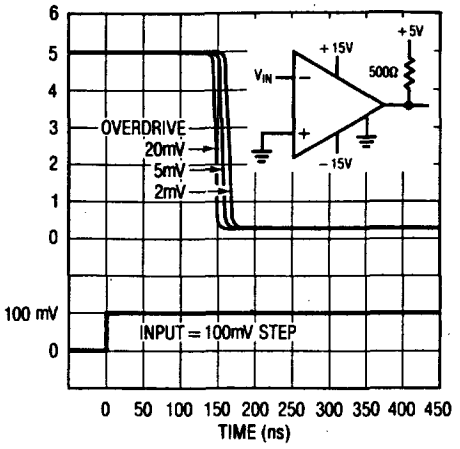
6

TYPICAL PERFORMANCE CHARACTERISTICS

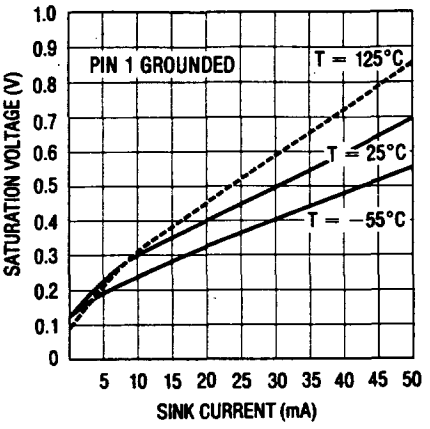
Response Time—Collector Output



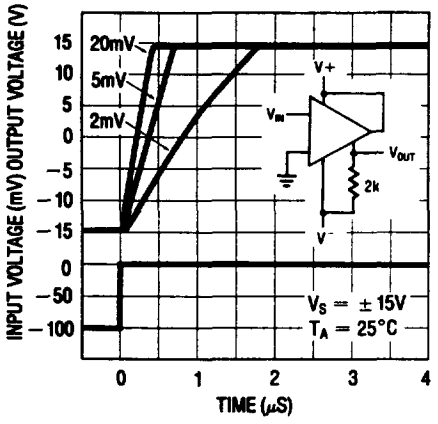
Response Time—Collector Output



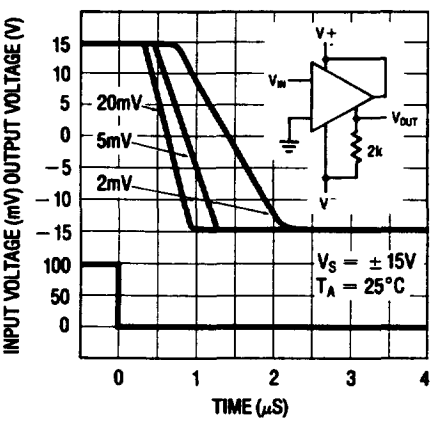
Collector Output Saturation Voltage



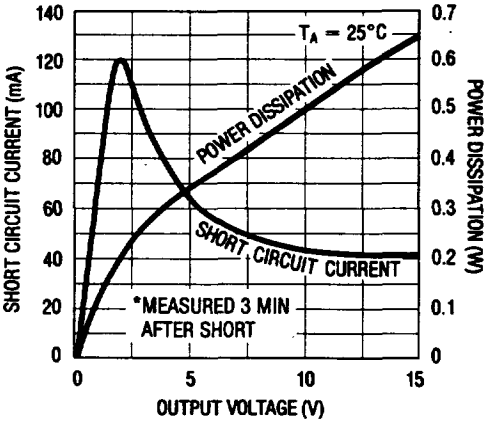
Response Time Using GND Pin as Output



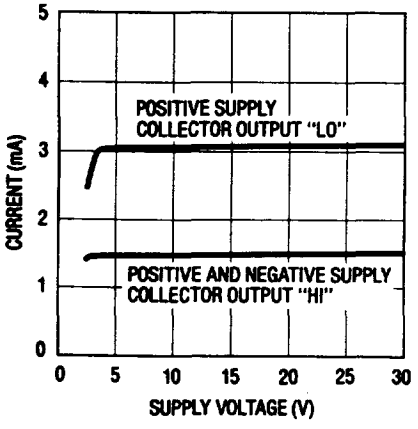
Response Time Using GND Pin as Output



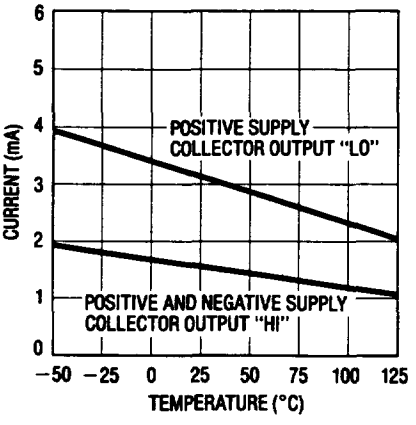
Output Limiting Characteristics*



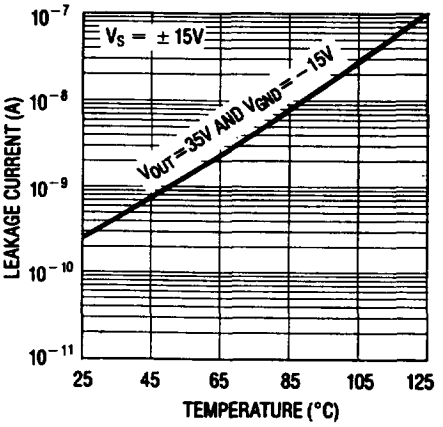
Supply Current vs Supply Voltage



Supply Current vs Temperature

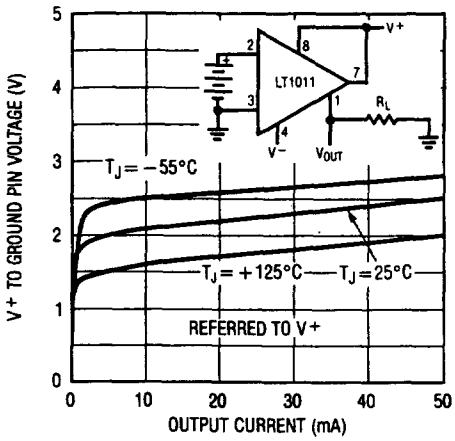


Output Leakage Current

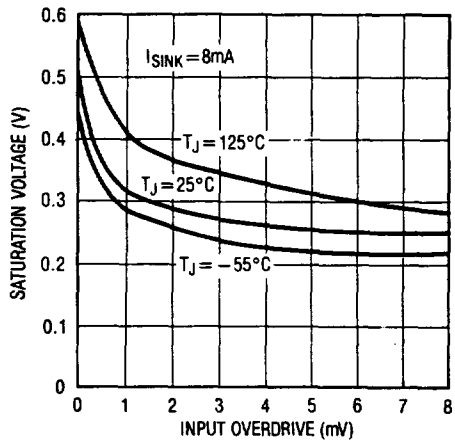


TYPICAL PERFORMANCE CHARACTERISTICS

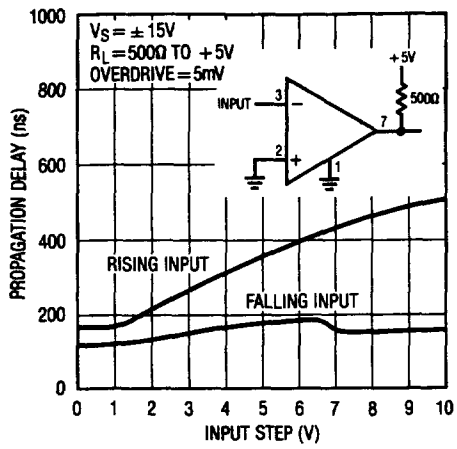
Output Saturation—Ground Output



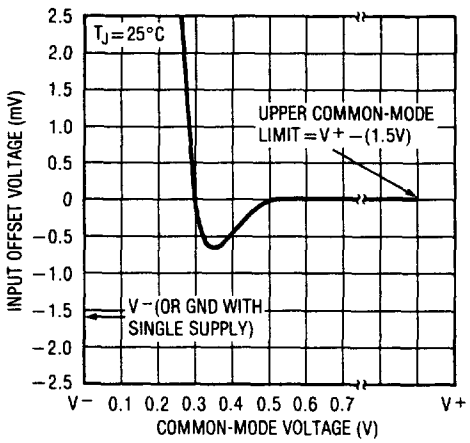
Output Saturation Voltage



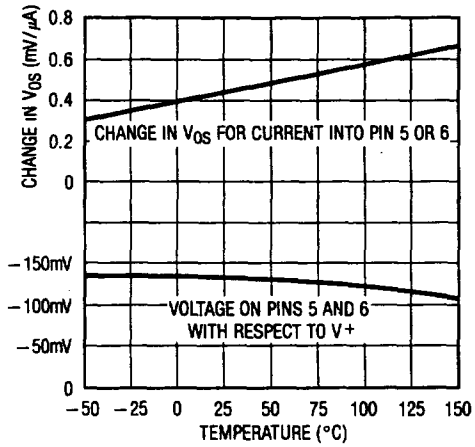
Response Time vs Input Step Size



Input Offset Voltage vs Common-Mode Voltage



Offset Pin Characteristics



6

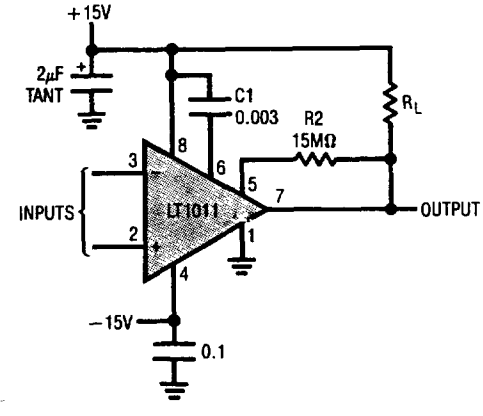
APPLICATIONS INFORMATION

Preventing Oscillation Problems

Oscillation problems in comparators are nearly always caused by stray capacitance between the output and inputs or between the output and other sensitive pins on the comparator. This is especially true with high gain-bandwidth comparators like the LT1011, which are designed for fast switching with millivolt input signal levels. The gain-bandwidth product of the LT1011 is over 10GHz. Oscillation problems tend to occur at frequencies around 5MHz, where the LT1011 has a gain of ≈2000. This implies that attenuation of output signals must be at least 2000:1 at 5MHz as measured at the inputs. If the source impedance is 1kΩ, the effective stray capacitance between output and input must have a reactance of more than (2000) (1kΩ) = 2MΩ, or less than 0.02pF. The actual interlead capacitance between input and output pins on the LT1011 is less than 0.002pF when cut to printed circuit mount length. Additional stray capacitance due to printed circuit traces must be minimized by routing the output trace directly away from input lines and, if possible, running ground traces next to input traces to provide shielding. Additional steps to ensure oscillation-free operation are:

1. Bypass the strobe/balance pins with a 0.01μF capacitor connected from pin 5 to pin 6. This eliminates stray capacitive feedback from the output to the balance pins, which are nearly as sensitive as the inputs.
2. Bypass the negative supply (pin 4) with a 0.1μF ceramic capacitor close to the comparator. 0.1μF can also be used for the positive supply (pin 8) if the pull-up load is tied to a separate supply. When the pull-up load is tied directly to pin 8, use a 2μF solid tantalum bypass capacitor.
3. Bypass any slow moving or DC input with a capacitor (≥0.01μF) close to the comparator to reduce high frequency source impedance.
4. Keep resistive source impedance as low as possible. If a resistor is added in series with one input to balance source impedances for DC accuracy, bypass it with a capacitor. The low input bias current of the LT1011 usually eliminates any need for source resistance balancing. A 5kΩ imbalance, for instance, will create only 0.25mV DC offset.
5. Use hysteresis. This consists of shifting the input offset voltage of the comparator when the output changes state. Hysteresis forces the comparator to move quickly through its linear region, eliminating oscillations by "overdriving" the comparator under all input conditions. Hysteresis may be either AC or DC. AC techniques do not shift the apparent offset voltage of the comparator, but require a *minimum* input signal slew rate to be effective. DC hysteresis works for all input slew rates, but creates a shift in offset voltage dependent on the previous condition of the input signal. The circuit shown below is an excellent compromise between AC and DC hysteresis.

Comparator with Hysteresis

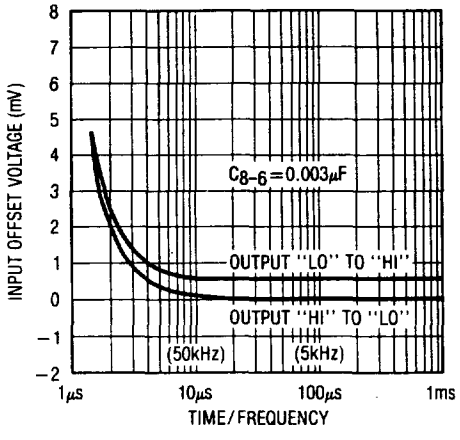


This circuit is especially useful for general purpose comparator applications because it does not force any signals directly back onto the input signal source. Instead, it takes advantage of the unique properties of the balance pins to provide extremely fast, clean output switching even with low frequency input signals in the millivolt range. The 0.003μF capacitor from pin 6 to pin 8 generates AC hysteresis because the voltage on the balance pins shifts slightly, depending on the state of the output. Both pins move about 4mV. If one pin (6) is bypassed, AC hysteresis is created. It is only a few millivolts referred to the inputs, but is sufficient to switch the output at nearly the maximum speed of which the comparator is capable. To prevent

APPLICATIONS INFORMATION

problems from low values of input slew rate, a slight amount of DC hysteresis is also used. The sensitivity of the balance pins to current is about 0.5mV input referred offset for each microampere of balance pin current. The 15mΩ resistor tied from output to pin 5 generates 0.5mV DC hysteresis. The combination of AC and DC hysteresis creates clean oscillation-free switching with very small input errors. The curve below plots input referred error versus switching frequency for the circuit as shown.

Input Offset Voltage vs Time to Last Transition

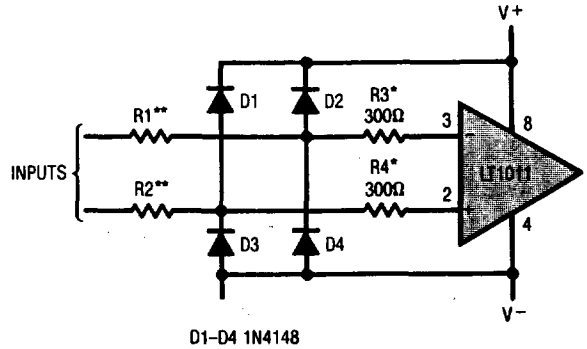


Note that at low frequencies, the error is simply the DC hysteresis, while at high frequencies, an additional error is created by the AC hysteresis. The high frequency error can be reduced by reducing C_H, but lower values may not provide clean switching with very low slew rate input signals.

Input Protection

The inputs to the LT1011 are particularly suited to general purpose comparator applications because large differential and/or common-mode voltages can be tolerated without damage to the comparator. Either or both inputs can be raised 40V above the negative supply, *independent of the positive supply voltage.* Internal forward biased diodes will conduct when the inputs are taken below the negative supply. In this condition, input current must be limited to 1mA. If very large (fault) input voltages must be accommodated, series resistors and clamp diodes should be used (see drawing below).

Limiting Fault Input Currents



D1–D4 1N4148
*MAY BE ELIMINATED FOR $I_{FAULT} \leq 1mA$
**SELECT ACCORDING TO ALLOWABLE FAULT CURRENT AND POWER DISSIPATION

The input resistors should limit fault current to a reasonable value (0.1mA to 20mA). Power dissipation in the resistors must be considered for continuous faults, especially when the LT1011 supplies are off. And one final caution: lightly loaded supplies may be forced to higher voltages by large fault currents flowing through D1–D4.

R3 and R4 limit input current to the LT1011 to less than 1mA when the input signals are held below V^-. They may be eliminated if R1 and R2 are large enough to limit fault current to less than 1mA.

Input Slew Rate Limitations

The response time of a comparator is typically measured with a 100mV step and a 5mV–10mV overdrive. Unfortunately, this does not simulate many real-world situations where the step size is typically much larger and overdrive can be significantly less. In the case of the LT1011, step size is important because the slew rate of internal nodes will limit response time for input step sizes larger than 1V. At 5V step size, for instance, response time increases from 150ns to 360ns. See the curve labeled Response Time vs Input Step Size for more detail.

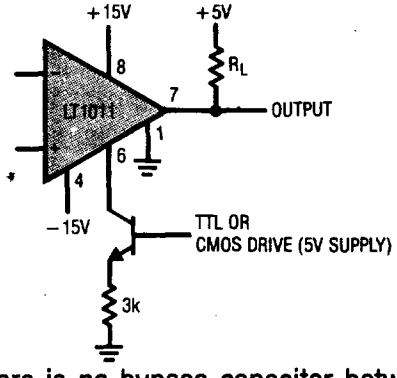
APPLICATIONS INFORMATION

If response time is critical and large input signals are expected, clamp diodes across the inputs are recommended. The slew rate limitation can also affect performance when differential input voltage is low, but both inputs must slew quickly. Maximum suggested common-mode slew rate is 10V/μs.

Strobing

The LT1011 can be strobed by pulling current out of the strobe pin. The output transistor is forced to an "off" state, giving a "hi" output at the collector (pin 7). Currents as low as 250μA will cause strobing, but at low strobe currents strobe delay will be 200ns–300ns. If strobe current is increased to 3mA, strobe delay drops to about 60ns. The voltage at the strobe pin is about 150mV below V^+ at zero strobe current and about 2V below V^+ for 3mA strobe current. *Do not ground the strobe pin. It must be current driven.* The drawing below shows a typical strobe circuit.

Typical Strobe Circuit



Note that there is no bypass capacitor between pins 5 and 6. This maximizes strobe speed, but leaves the comparator more sensitive to oscillation problems for slow, low level inputs. A 1pF capacitor between the output and pin 5 will greatly reduce oscillation problems without reducing strobe speed.

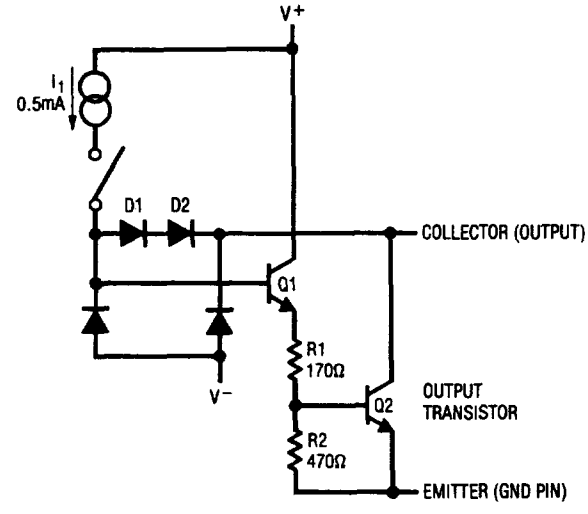
DC hysteresis can also be added by placing a resistor from output to pin 5. See step number 5 under "Preventing Oscillation Problems".

The pin (6) used for strobing is also one of the offset adjust pins. Current flow into or out of pin 6 must be kept very low ($<0.2\mu$A) when not strobing to prevent input offset voltage shifts.

Output Transistor

The LT1011 output transistor is truly floating in the sense that no current flows into or out of either the collector or emitter when the transistor is in the "off" state. The equivalent circuit is shown in the drawing below.

Output Transistor Circuitry



In the "off" state, I_1 is switched off and both Q1 and Q2 turn off. The collector of Q2 can be now held at any voltage above V^- without conducting current, including voltages above the positive supply level. Maximum voltage above V^- is 50V for the LT1011 and 40V for the LT1011C. The emitter can be held at any voltage between V^+ and V^- as long as it is negative with respect to the collector.

In the "on" state, I_1 is connected, turning on Q1 and Q2. Diodes D1 and D2 prevent deep saturation of Q2 to improve speed and also limit the drive current of Q1. The R1/R2 divider sets the saturation voltage of Q2 and provides turn-off drive. Either the collector or emitter pin can be held at a voltage between V^+ and V^-. This allows the remaining pin to drive the load. In typical applications, the emitter is connected to V^- or ground and the collector drives a load tied to V^+ or a separate positive supply.

APPLICATIONS INFORMATION

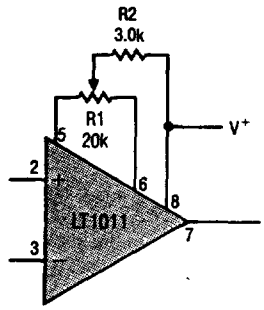
When the emitter is used as the output, the collector is typically tied to V^+ and the load is connected to ground or V^-. Note that the emitter output is phase reversed with respect to the collector output so that the "+" and "−" input designations must be reversed. When the collector is tied to V^+, the voltage at the emitter in the "on" state is about 2V below V^+ (see curves).

Input Signal Range

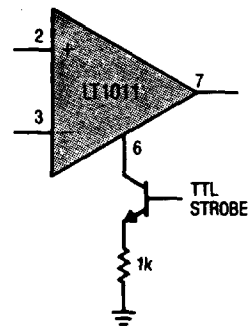
The common-mode input voltage range of the LT1011 is about 300mV above the negative supply and 1.5V below the positive supply, independent of the actual supply voltages (see curve in typical performance characteristics). This is the voltage range over which the output will respond correctly when the common-mode voltage is applied to one input and a higher or lower signal is applied to the remaining input. *If one input is inside the common-mode range and one is outside, the output will be correct. If the inputs are outside the common-mode range in opposite directions, the output will still be correct. If both inputs are outside the common-mode range in the same direction, the output will not respond to the differential input; it will remain unconditionally high* (collector output).

TYPICAL APPLICATIONS

Offset Balancing

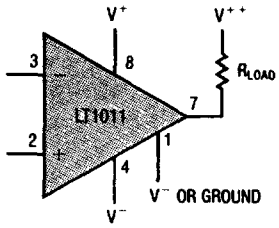


Strobing



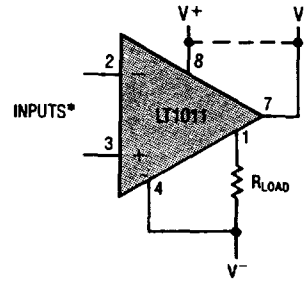
NOTE: DO NOT GROUND STROBE PIN.

Driving Load Referenced to Positive Supply



V^{++} CAN BE GREATER OR LESS THAN V^+

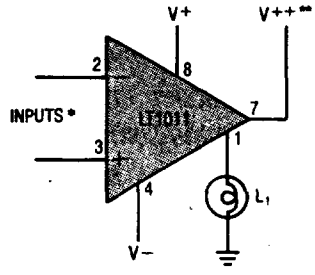
Driving Load Referenced to Negative Supply



* INPUT POLARITY IS REVERSED WHEN USING PIN 1 AS OUTPUT

TYPICAL APPLICATIONS

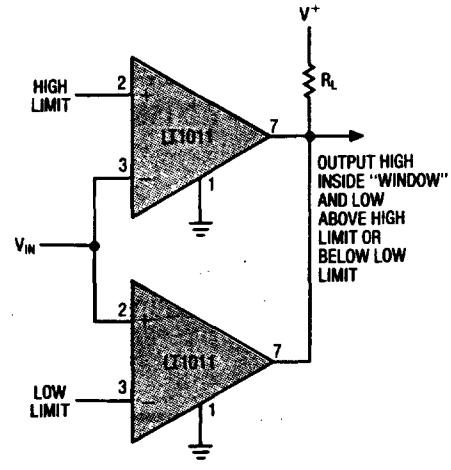
Driving Ground Referred Load



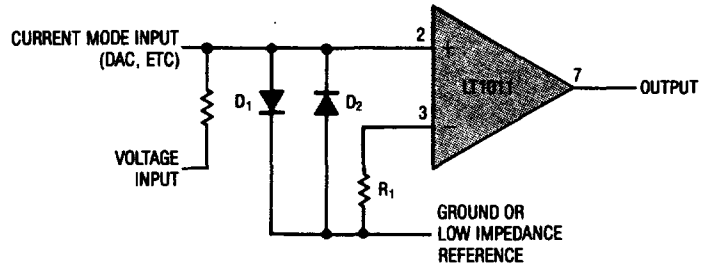
* INPUT POLARITY IS REVERSED WHEN USING PIN 1 AS OUTPUT

**V++ MAY BE ANY VOLTAGE ABOVE V−. PIN 1 SWINGS TO WITHIN ≈2V OF V++.

Window Detector

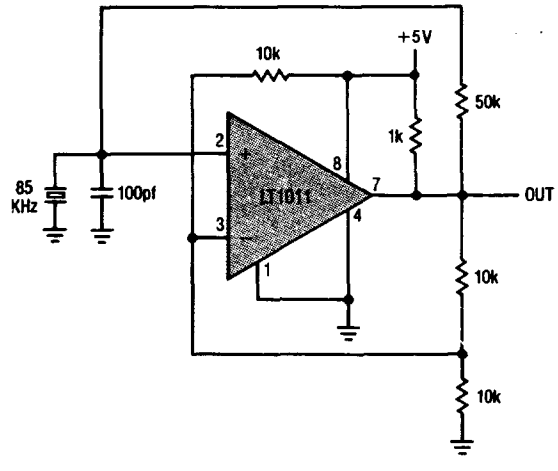


Using Clamp Diodes to Improve Frequency Response*



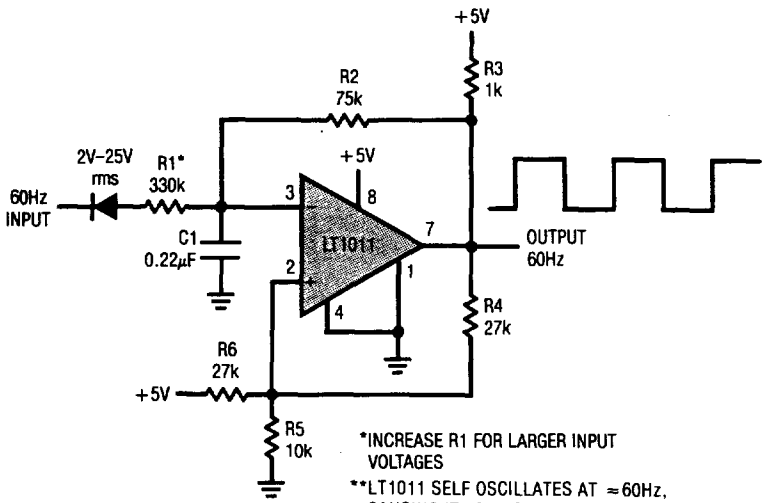
*SEE CURVE, "RESPONSE TIME VS INPUT STEP SIZE"

Crystal Oscillator



TYPICAL APPLICATIONS

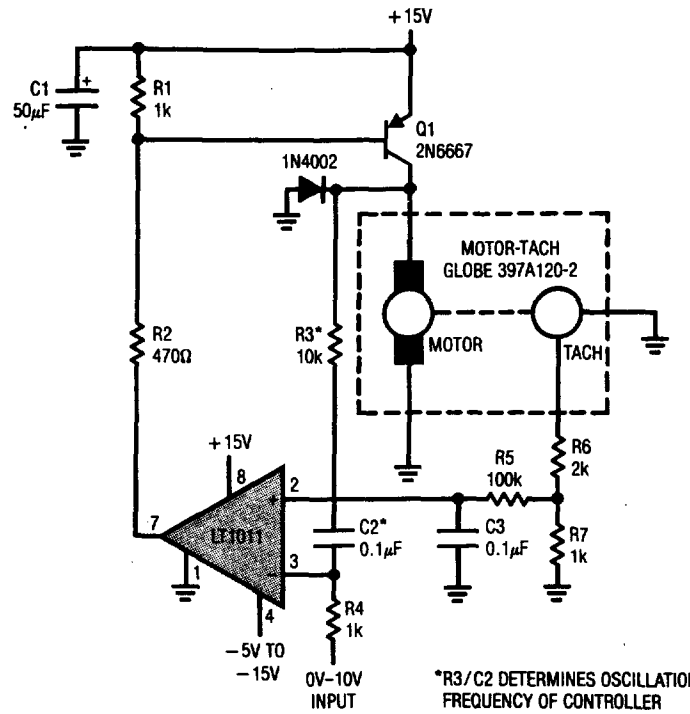
Noise Immune 60Hz Line Sync**



*INCREASE R1 FOR LARGER INPUT VOLTAGES

**LT1011 SELF OSCILLATES AT ≈60Hz, CAUSING IT TO "LOCK" ON TO INCOMING LINE SIGNAL.

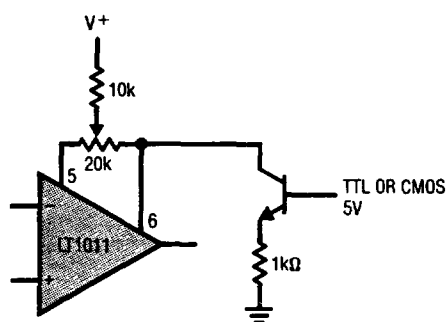
High Efficiency**Motor Speed Controller



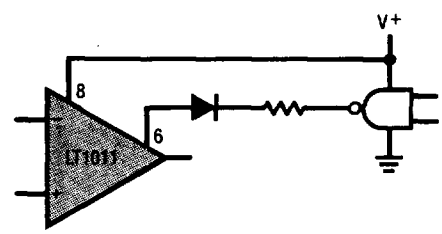
*R3/C2 DETERMINES OSCILLATION FREQUENCY OF CONTROLLER

**Q1 OPERATES IN SWITCH MODE

Combining Offset Adjust and Strobe

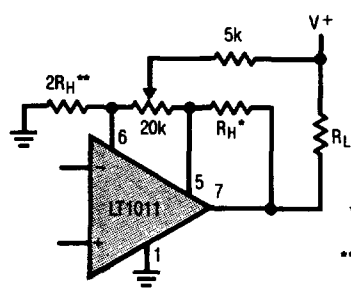


Direct Strobe Drive when CMOS* Logic Uses Same V+ Supply as LT1011



*NOT APPLICABLE FOR TTL LOGIC

Combining Offset Adjustment and Hysteresis

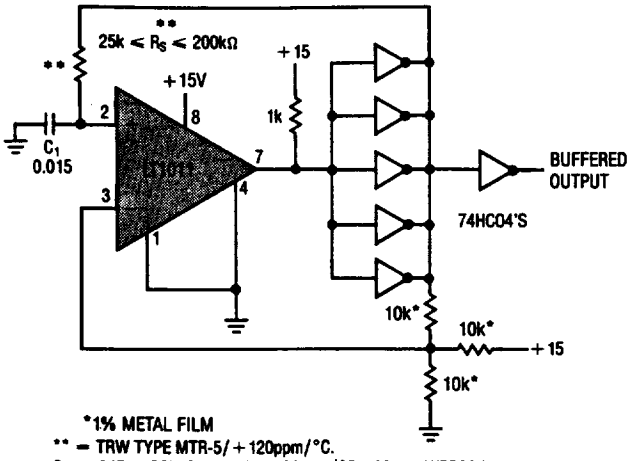


*HYSTERESIS IS ≈0.45mV/μA OF CURRENT CHANGE IN R_H

**THIS RESISTOR CAUSES HYSTERESIS TO BE CENTERED AROUND V_{OS}

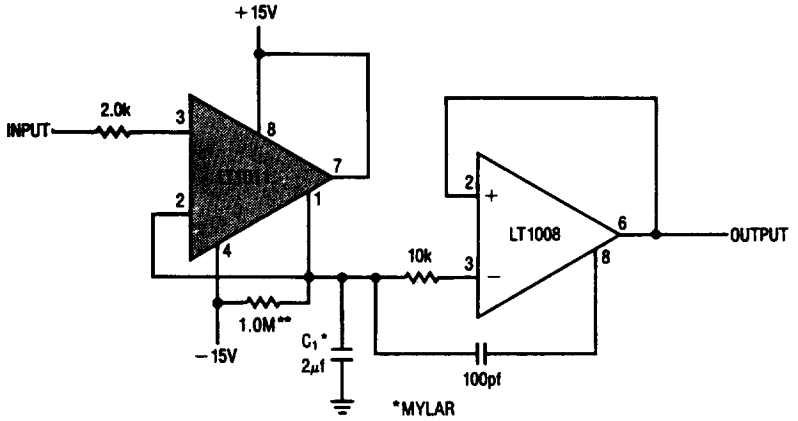
TYPICAL APPLICATIONS

Low Drift R/C Oscillator†



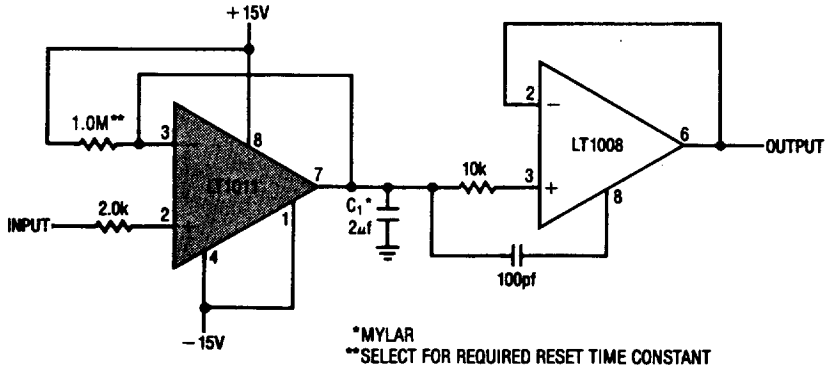
*1% METAL FILM
** = TRW TYPE MTR-5/+120ppm/°C.
C_1 = .015 = POLYSTYRENE −120ppm/°C ± 30ppm WESCO TYPE 32-P
NOTE: COMPARATOR CONTRIBUTES ≤ 10ppm/°C DRIFT FOR FREQUENCIES BELOW 10kHz.
†LOW DRIFT AND ACCURATE FREQUENCY ARE OBTAINED BECAUSE THIS CONFIGURATION REJECTS EFFECTS DUE TO INPUT OFFSET VOLTAGE AND BIAS CURRENT OF THE COMPARATOR.

Positive Peak Detector



*MYLAR
**SELECT FOR REQUIRED RESET TIME CONSTANT

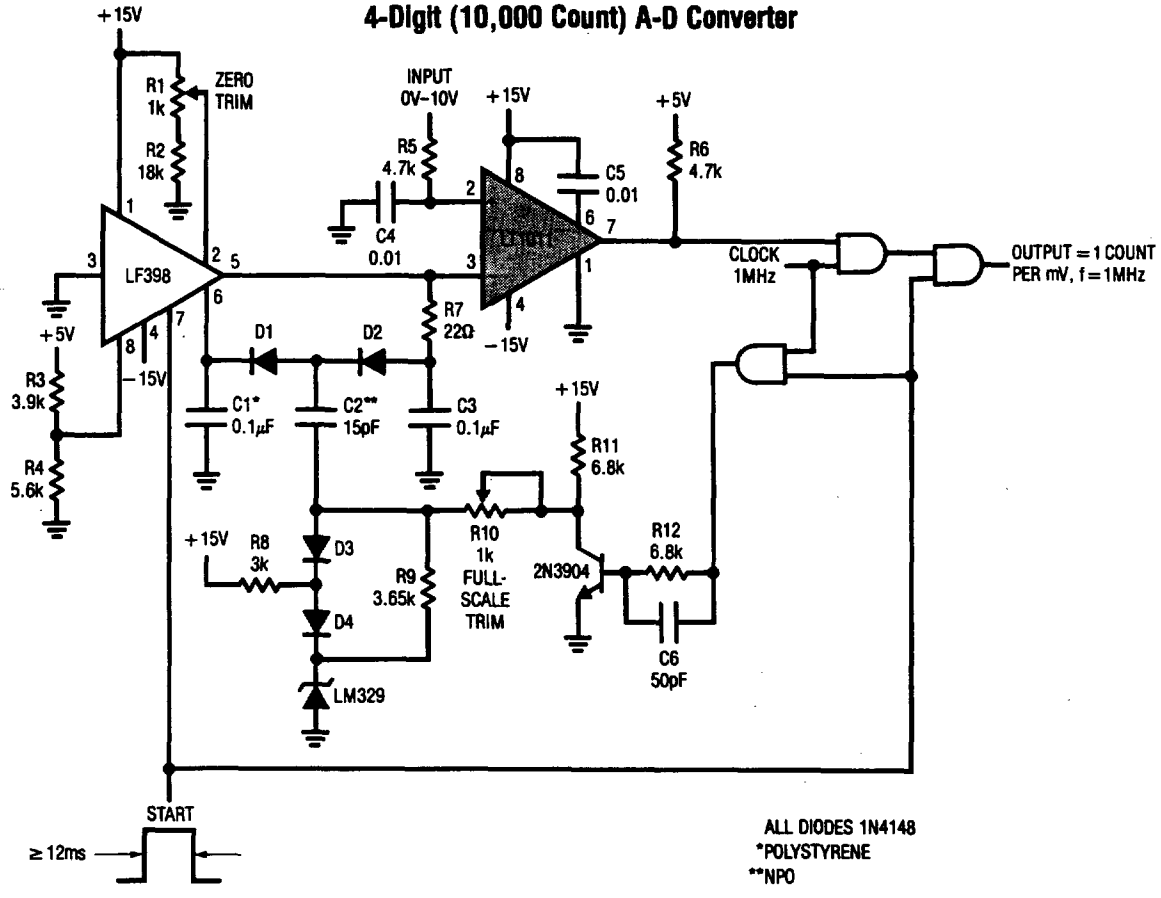
Negative Peak Detector



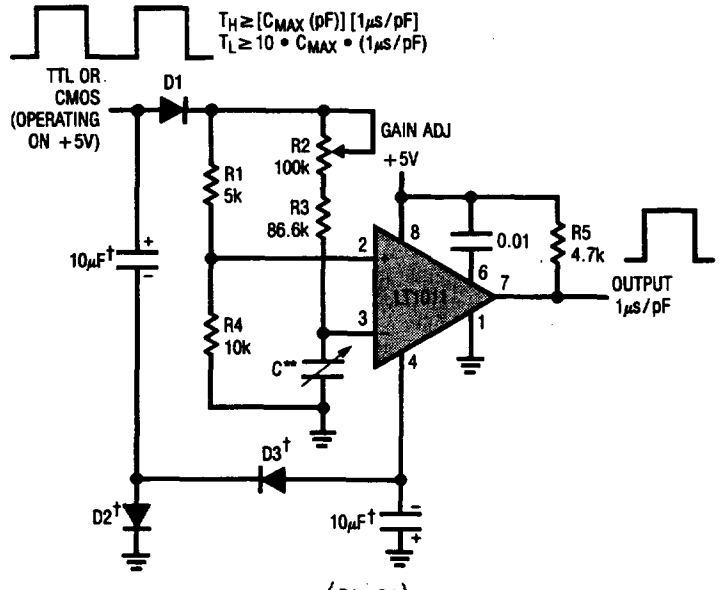
*MYLAR
**SELECT FOR REQUIRED RESET TIME CONSTANT

TYPICAL APPLICATIONS

4-Digit (10,000 Count) A-D Converter



Capacitance to Pulse Width Converter



*$PW = (R2 + R3)\ (C)\left(\frac{R1 + R4}{R1}\right)$, INPUT CAPACITANCE OF LT1011 IS ≈6pF. THIS IS AN OFFSET TERM.

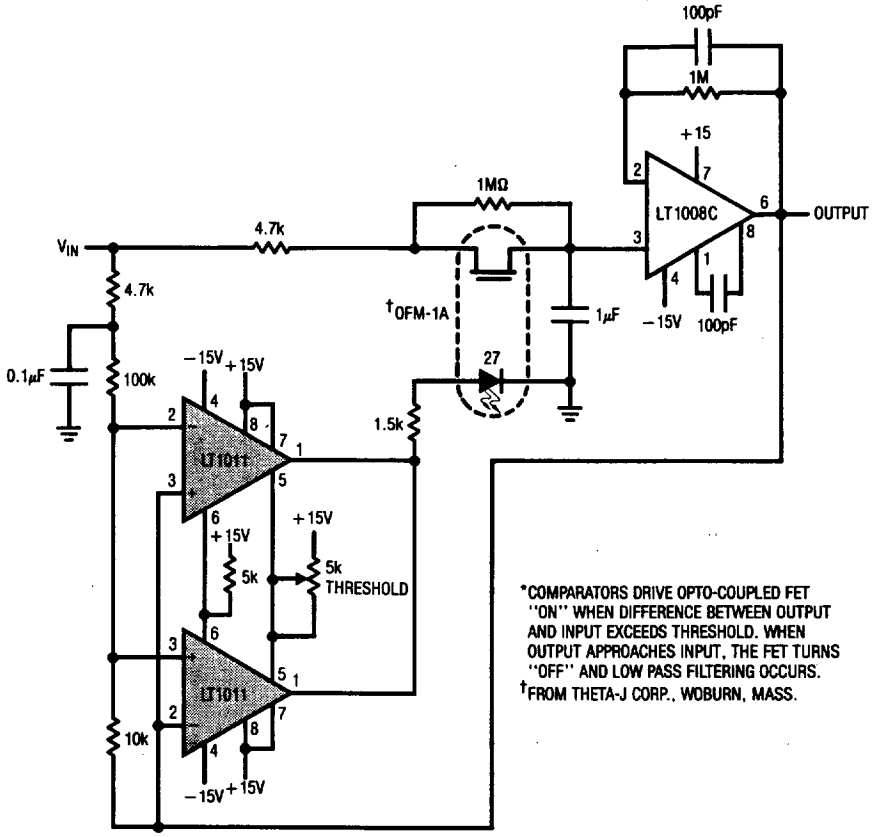
†THESE COMPONENTS MAY BE ELIMINATED IF NEGATIVE SUPPLY IS AVAILABLE (−1V TO −15V).

**TYPICAL 2 SECTIONS OF 365pF VARIABLE CAPACITOR WHEN USED AS SHAFT ANGLE INDICATION.

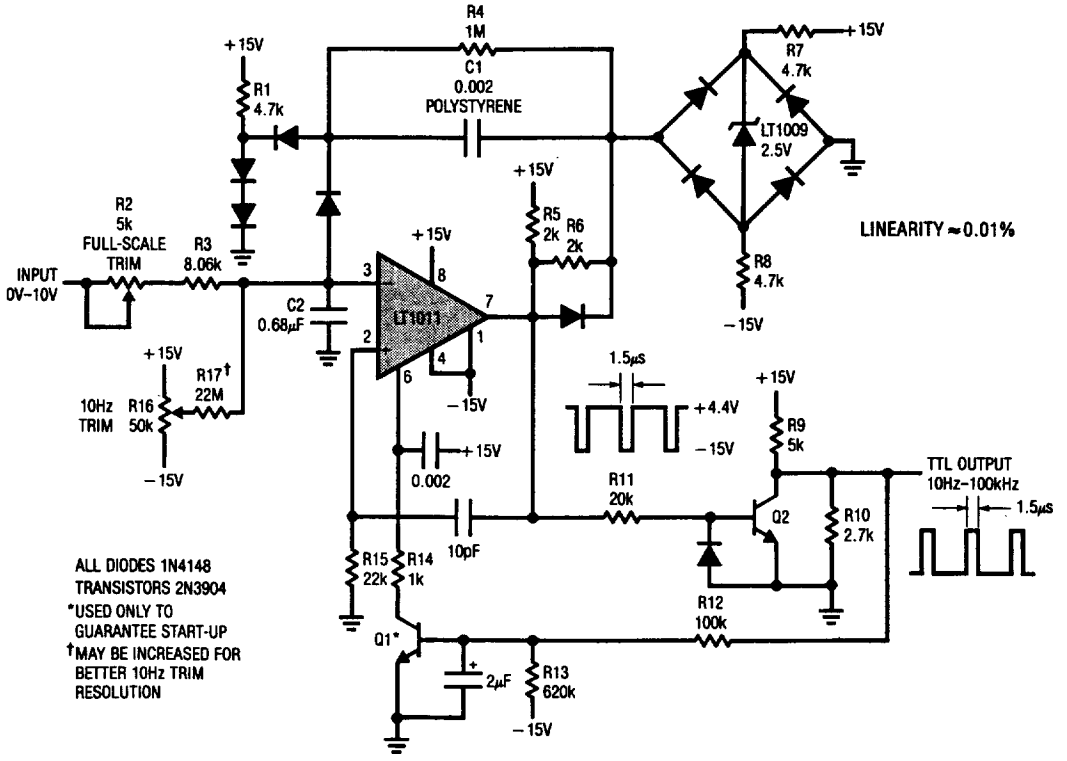
6

TYPICAL APPLICATIONS

Fast Settling* Filter

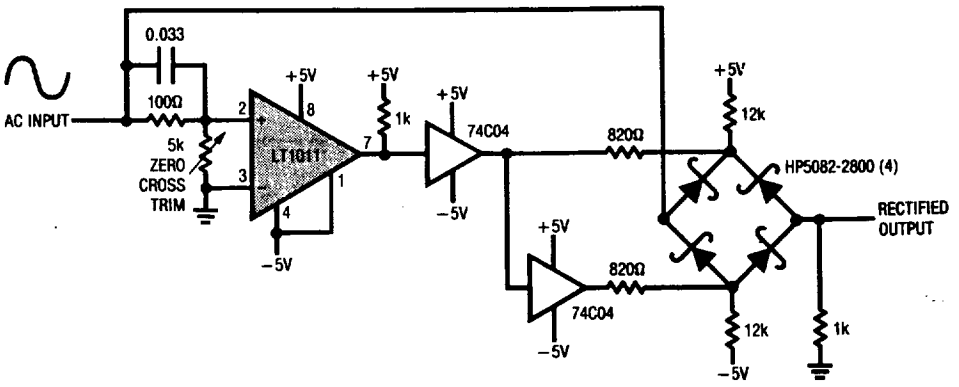


10Hz to 100kHz Voltage to Frequency Converter

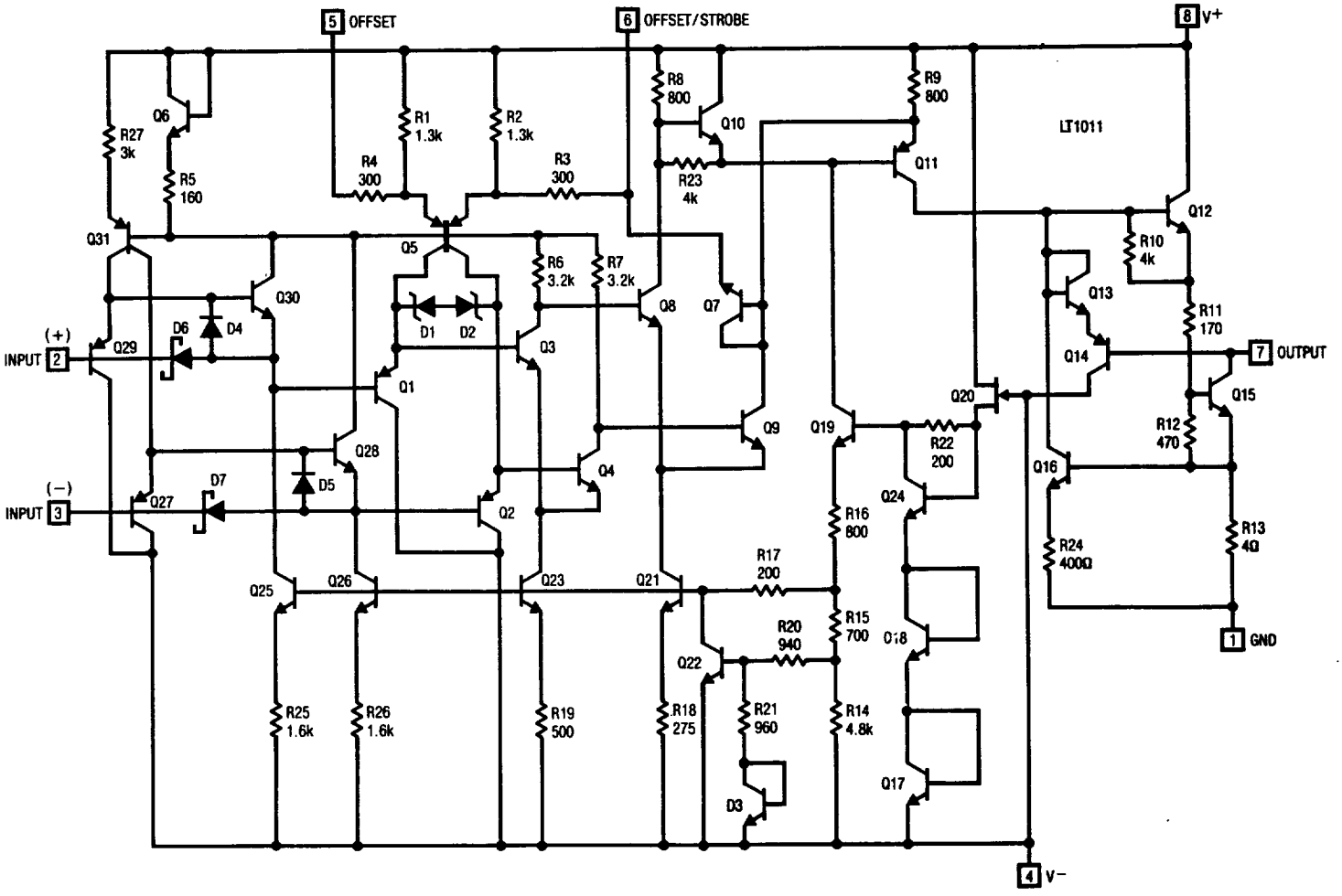


TYPICAL APPLICATIONS

100kHz Precision Rectifier

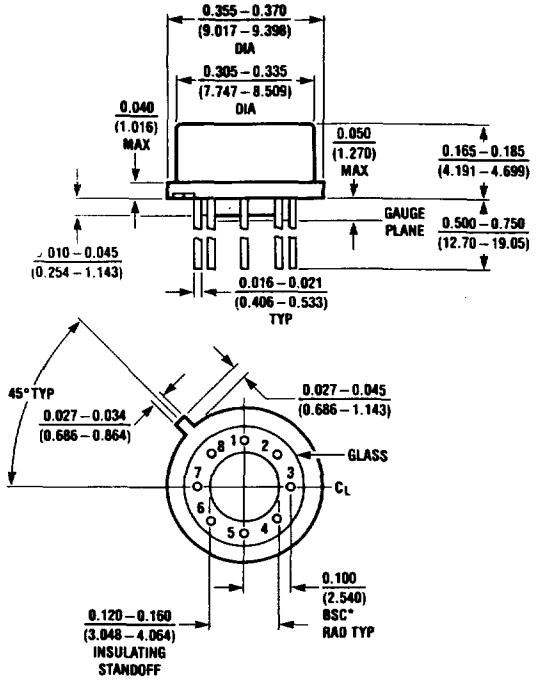


SCHEMATIC DIAGRAM



PACKAGE DESCRIPTION

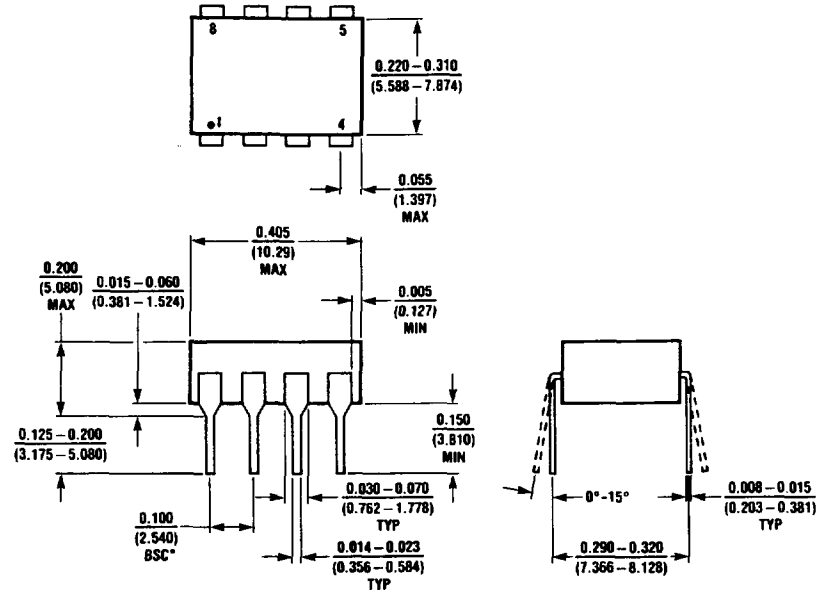
H Package
Metal Can



NOTE: DIMENSIONS IN INCHES

$T_j$max	θ_{ja}	θ_{jc}
150°C	150°C/W	45°C/W

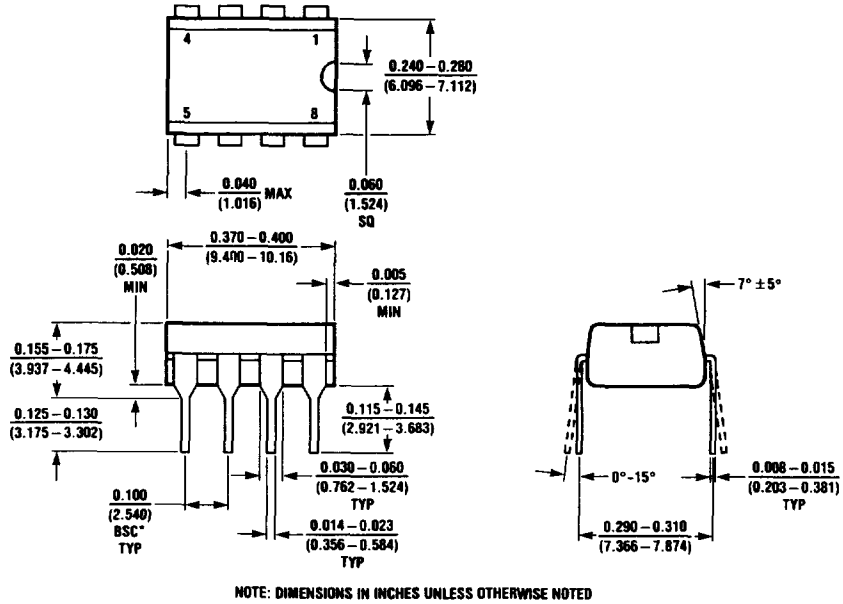
J8 Package
8 Lead Hermetic DIP



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

$T_j$max	θ_{ja}
150°C	100°C/W

N8 Package
8 Lead Plastic



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

$T_j$max	θ_{ja}
100°C	130°C/W